* S F - 6 5 2 9 / 1 0 0 *

SF-6529

B. E. - II (Sem. IV) (IC) Examination

May / June - 2011

Digital Integrated Circuits

Time : **3** Hours] [Total Marks : **100**

Instructions :

(1)

નીચે દર્શાવેલ ☛ નિશાનીવાળી વિગતો ઉત્તરવહી પર અવશ્ય લખવી.
Fillup strictly the details of ☛ signs on your answer book.

Name of the Examination :

☛ B. E. - 2 (SEM. 4) (IC)

Name of the Subject :

☛ DIGITAL INTEGRATED CIRCUITS

☛ Subject Code No. : 6 5 2 9 ☛ Section No. (1, 2,.....) : 1&2

Seat No. :

Student's Signature

(2) Attempt all questions.
(3) Figures to the right indicates the marks.
(4) Assume suitable data whenever necessary.
(5) Answer to the two sections must be written in separate answer book.

SECTION - I

1 (a) Attempt any four : **12**

(i) Explain "FANOUT".
(ii) "DTL is faster than TTL". True or False? Justify.
(iii) Draw and explain circuit of TTL inverter.
(iv) What is a function of diode connected between inputs and Ground in TTL ?
(v) Explain term : Saturated Logic and Non Saturated Logic.

(b) Attempt any two : **8**

(i) Explain current hogging in DCTL.
(ii) Draw and explain basic gate with multi emitter transistor.
(iii) Draw and explain fabrication of Schottky transistor.

2 (a) Explain Physical Layout of IIL. **7**

(b) Explain Transfer Characteristic of ECL gate. **7**

OR

(b) Discuss Manufacturing Specification of RTL gates. **7**

3 Attempt any two : **16**

(i) Explain in detail Types of TTL Gates.

(ii) Define Operating Voltages : VOH, VOL, VIL, VIH.

(iii) Explain High threshold DTL Gate.

SECTION - II

4 (a) Answer the following questions : **10**

(i) Give example of SSI and MSI ICs.

(ii) Where information can be stored in EPROM Cell ?

(iii) What is negative logic gate ?

(iv) How the information is stored in six-transistor static cell ?

(v) Define : Dynamic memory.

(b) Discuss fall time in MOS gate. **6**

(c) Discuss average power dissipation and delay power production for CMOS inverter. **4**

5 (a) Discuss working of EPROM in detail and compare it with EEPROM. **8**

(b) Discuss the organization of a memory for a M-word 3 bit/word memory. **7**

OR

5 (a) Discuss the Programmable logic array with proper example. PLA is consisting programmable AND and Programmable OR arrays. **8**

(b) Explain the shift Register with the help of MOS gate. **7**

6 Answer any three :

(i) Explain BJT-CMOS interfacing. Why and where does the pull up register require ?

(ii) In connection with conventional BICMOS inverter and improve your design with passive to actie discharging device.

(iii) Discuss the Decoder ROM and A three-word, 5 bit ROM using diode connection between address lines and bit lines.

(iv) Compare PMOS and NMOS and write the Active and Saturation Current Equation.

(v) Discuss shift register sequential memory.
